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Description

METHOD FOR ANALYZING DEFECT INSPECTION PARAMETERS

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method for analyzing process parameters, and more particularly, to a method for analyzing defect inspection parameters.

[0003] 2. Description of the Prior Art

[0004] In a semiconductor manufacturing technique, many processes, such as the photolithography processes, the etching processes, and the ion implantation processes are required to complete the fabrication of a semiconductor product. That means a large number of equipment and complicated procedures are utilized in a semiconductor manufacturing process. Therefore, those of ordinary skill in the art are concentrated on ensuring the proper operation of equipment, sustaining or improving production

yield rate, detecting and verifying problems, and periodically maintaining facilities for production, etc, so as to maintain the company"s operation in good progress and produce products having good quality.

[0005] In order to identify the semiconductor processing problems, the following data, such as the process parameter data, the in-line quality control (in-line QC) data, the defect inspection data, the sample test data, the wafer test data, and the final test data, are analyzed. The defect inspection data is acquired by inspecting the defects in each layer on the wafer. The defect inspection data includes the total count of defects, the adder count of defects, and the class count of defects. The data obtained from defect inspection is usually represented by a defect distribution map.

[0006] Please refer to Fig.1. Fig.1 is a flow chart of a prior art method for analyzing defect inspection parameters. As shown in Fig.1, step 101 is first executed by those of ordinary skill in the art to perform inspection according to various defect inspection items to each wafer. For example, the total count of defects in an intermetal dielectric layer is inspected.

[0007] Step 102 is thereafter executed to find out the products

having abnormal defect inspection results by reviewing the results of each defect inspection item of each wafer. Please refer to Fig.2. Fig.2 is a schematic diagram of a defect inspection parameter distribution map for a wafer. As shown in Fig.2, a wafer is divided into a plurality of dies 21. A plurality of black dots represent the sites of defects 22 occurring in a specific layer on the wafer.

[0008] In step 103, those of ordinary skill in the art determine the possibly faulty process step according to personal experience and the defect distribution maps of abnormal products obtained from step 102. For example, the possibly faulty process step may be a process step for forming a polysilicon layer, a metal layer, an intermetal dielectric layer, etc.

[0009] Finally, those of ordinary skill in the art find out the ill-functioned equipment by checking the equipment utilized in the process step determined in step 103. For example, those of ordinary skill in the art judge that the products are out of spec according to the total count of defects in the intermetal dielectric layer first, then determine the possibly faulty process step to be the intermetal dielectric layer deposition process step, and eventually find out the ill-functioned equipment, such as the depositing equip-

ment, the etching equipment, etc.

[0010] Since the analysis results are determined according to humans experience (step 103) in the prior art, the accuracy and the confidence level of the final analysis results are open to question. Furthermore, the human affairs in semiconductor manufacturing change frequently. Engineer"s personal experience is difficult to transfer. The capacity of each engineer is limited,meaning the engineer is unable to look after the operation status of all of the equipment. When the defect inspection results indicate abnormalities, it is thus difficult for engineers, lacking in experience, to judge which point causes the problem to occur. Therefore, a lot of time is consumed to do related research, and even worse, wrong decisions are made. This will not only reduce the efficiency of processes, but also increase the cost, Furthermore, the in-line production status can not be improved in time to increase yield rate.

[0011] It is therefore very important to provide an analytical-method to rapidly and correctly judge which point causes the problem to occur when the defect inspection data of semiconductor products indicates abnormalities.

SUMMARY OF INVENTION

[0012] It is a primary objective of the claimed invention to pro-

vide a method for analyzing defect inspection parameters to rapidly and correctly judge which point causes the problem to occur when the defect inspection data of semiconductor products indicates abnormalities.

[0013] It is another primary objective of the claimed invention to provide a method for analyzing defect inspection parameters to revise the kill ratio of the defect inspection according to the results of defect inspection and wafer test.

[0014] It is a feature of the claimed invention to utilize the commonality analysis means to analyze defect inspection parameters by coordinating with the database recording each defect inspection item and correlated processing equipment.

[0015] The claimed invention method for analyzing defect inspection parameters are utilized for analyzing a plurality of lots of products. Each of the plurality of lots of products has a lot number. The plurality of lots of products are fabricated through a plurality of manufacturing equipment. At least one wafer in each of the plurality of lots of products is inspected according to at least one defect inspection item to generate at least one defect inspection parameter. The defect inspection item, the defect inspection parameter, and a process step correlated to the de-

fect inspection item are stored in a database. The method includes: searching for the defect inspection parameters of the plurality of lots of products from the database, classifying the plurality of lots of products into at least a qualified group and a failed group according to the defect inspection parameters, searching for the process step correlated to the defect inspection item from the database, searching for the manufacturing equipment through which the qualified group has passed in the process step and the manufacturing equipment through which the failed group has passed in the process step, and determining the manufacturing equipment through which the probability that the failed group has passed which is greater than that of the qualified group.

[0016] Each wafer of each lot of products is tested according to a wafer test item correlated to the defect inspection item to generate a wafer test parameter. The wafer test item and the wafer test parameter are stored in the database. The present invention method for analyzing defect inspection parameters utilizes the overlapping means to compare the wafer test parameter distribution map and the defect distribution map to find out optimum kill ratio of the defect inspection.

[0017] It is an advantage of the claimed invention to utilize the commonality analysis means to analyze the defect inspection parameters by coordinating with the database recording each defect inspection item and related processing equipment. Therefore, the point causing the problem to occur is judged rapidly and correctly to find out the ill-functioned equipment when the defect inspection data of semiconductor products indicates abnormalities. Furthermore, the kill ratio of the defect inspection is revised according to the results of defect inspection and wafer test to avoid mistakes incurred from human"s judgment, leading to higher processing efficiency, lower cost, and better in-line production status control to increase yield rate.

[0018] These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of Drawings

[0019] Fig.1 is a flow chart of a prior art method for analyzing defect inspection parameters.

[0020] Fig.2 is a schematic diagram of a defect inspection pa-

rameter distribution map for a wafer.

[0021] Fig.3 is a flow chart of a method for analyzing defect inspection parameters according to a preferred embodiment of the present invention.

[0022] Fig.4 and Fig.5 areflow charts of a method for analyzing defect inspection parameters according to another preferred embodiment of the present invention.

[0023] Fig.6 is a schematic diagram of a wafer test parameter distribution map according to another preferred embodiment of the present invention.

DETAILED DESCRIPTION

[0024] In the following, relevant figures are referred to illustrate the method for analyzing the defect inspection parameters according to a preferred embodiment of the present invention. The same components are narrated with the same reference symbols.

[0025] Please refer to Fig.3. Fig.3 is a flow chart of a method for analyzing defect inspection parameters according to the preferred embodiment of the present invention. The method is used for rapid and correct judging which equipment causes the problem to occur when the defect inspection data of semiconductor products indicates abnormalities.

[0026] As shown in Fig.3, step 301 is first executed to search for the defect inspection parameters of a plurality of lots of products. Each lot of products, having a lot number, includes twenty-five pieces of wafers. Each lot of products is fabricated through a plurality of equipment of a plurality of process steps. At least one wafer in each lot of products is inspected according to at least one defect inspection item to generate at least one defect inspection parameter. In the preferred embodiment of the present invention, the defect inspection results can be classified into the total count of defects, the adder count of defects, and the class count of defects. The defect inspection parameters may be represented by a defect distribution map. For example, the defect distribution map for the adder count of defects is shown in Fig.2. Each of a plurality of black dots, distributed over a plurality of dies 21 on the wafer, respectively represents a defect 22. It is worth noticing that defects may occur in different layers on the wafer to result in more than one defect distribution map for one wafer.

[0027] Step 302 is thereafter executed to demonstrate the defect inspection results of each lot of products with charts. In the preferred embodiment of the present invention, a his-

togram chart is utilized to represent the defect inspection parameters, such as the total count of defects, the adder count of defects, and the class count of defects, of each lot of products. Byobserving the histogram chart, engineers are able to realize the defect inspection parameter distribution.

[0028] In step 303, the plurality of lots of products acquired in step 301 are classified into at least two groups. The classifying criterion is whether each of the defect inspection parameters is within the predefined spec or not. The plurality of lots of products are classified into a qualified group and a failed group. According to the preferred embodiment of the present invention, the plurality of lots of products whose defect inspection parameters are within the predefined spec are classified as group A (qualified group). For example, the products from lots numbers 1, 2, 3, 4, and 5 are classified as group A (as shown in step 304). The plurality of lots of products whose defect inspection parameters are not within the predefined spec are classified as group B (failed group). For example, the products from lots numbers 6, 7, 8, 9, and 10 are classified as group B (as shown in step 305).

[0029] After that, step 306 is executed to search for the process

steps correlated to the specific layers inspected according to the defect inspection items from another database set up from accumulative experience. For example, if the defect inspection items are performed on an intermetal dielectric layer, the correlated process steps can be the process step for depositing the dielectric layer after the first metal layer, the photolithography process step, or the etching process step. In the preferred embodiment of the present invention, the database set up from accumulative experience includes the experience of senior engineer acquired from problem tracing and the data derived from the computer system according to the present invention method.

[0030] Step 307 is executed to trace out a specific process step after the process steps correlated to the specific layers inspected according to the defect inspection items are acquired from the database, set up from accumulative experience, in step 306.

[0031] Step 308 is then executed to search for the equipment through which the traced process step is performed. For example, equipment numbers E1, E2, E3, etc. are acquired. Step 309 is thereafter executed to calculate the probability of each of the equipment through which the

Group B has passed in the process step, and Step 310 is executed to calculate the probability of each of the equipment through which the Group A has passed. Finally, Step 311 is executed to determine the equipment through which the probability that the group B has passed which is greater than that of the group A, by utilizing the commonality analysis means. The equipment through which the probability that the group B has passed which is greater than that of the group A, determined in Step 311, is the possibly faulty equipment analyzed according to the analytical method for the defect inspection parameters in the preferred embodiment of the present invention.

[0032] Please refer to Fig.4 and Fig.5. Fig.4 and Fig.5 areflow charts of a method for analyzing defect inspection parameters according to another preferred embodiment of the present invention. This method is used for revising the criterion for defect quantity according to defect distribution and wafer test results. According to this preferred embodiment of the present invention, each wafer in each lot of products is inspected according to a wafer test item to generate a wafer test parameter. The wafer test items, the wafer test parameters, and the correlation between the defect inspection items and the wafer test items are

stored in a database.

[0033] As shown in Fig.4 and Fig.5, step 401 is first executed to search for the defect inspection parameters of a plurality of lots of products. As mentioned previously, each lot of products, having a lot number, includes twenty-five pieces of wafers. At least one wafer in each lot of products is inspected according to the defect inspection item, and each wafer is tested according to the wafer test item. Therefore, the defect inspection parameters and the wafer test parameters are generated. In this preferred embodiment of the present invention, the defect inspection parameters may be represented by a defect distribution map (as shown in Fig.2). Each of a plurality of black dots, distributed over a plurality of dies 21 on the wafer, respectively represents a defect 22. The dies having black dot inside are defective dies 23. It is worth noticing that defects may occur in different layers on the wafer to result in more than one defect distribution map for one wafer.

[0034] Step 402 is thereafter executed to determine whether the defect inspection parameters of each lot of products, acquired in Step 401, exceed the predefined spec or not. Generally speaking, the predefined spec for the defect inspection parameters is a range. In this step, whether the

acquired defect inspection parameters of each lot of products exceed the predefined upper control limit (UCL) or not is judged. In addition, the defect inspection item analyzed in this step may be the total count of defects, the adder count of defects, and the class count of defects. According to this preferred embodiment of the present invention, each wafer in each lot of products is searched in Step 402. If the defect inspection parameters of more than one wafer in one lot of products exceed the predefined spec, then execute Step 403 to select the lot number of that lot. If not, stop analyzing. After that, Step 404 is executed to acquire the defect inspection parameter distribution map for the defective wafer.

[0035] Step 405 is then executed to judge whether the wafer test parameters of that lot of products, whose lot number was selected in Step 403, are stored in the database or not. In this preferred embodiment of the present invention, the wafer test parameters can be represented by a wafer test parameter distribution map. Please refer to Fig.6. Fig.6 is a schematic diagram of a wafer test parameter distribution map according to another preferred embodiment of the present invention. As shown in Fig.6, a wafer is divided into a plurality of dies including a plurality of failed

dies 51 (indicated with black color) and a plurality of qualified dies 52 (indicated with white color). If the wafer test parameters are stored in the database according to the judgment made in Step 405, Step 406 is executed to acquire the wafer test parameter distribution map for each wafer in that lot of products. If not, stop analyzing. It is worth noticing that the wafer test parameters searched and analyzed in Steps 405, 406 are testing results of wafer test items correlated to defect inspection items, such as results of the function test item and the I_{DDQ} test item.

[0036] After that, Step 407 is executed to compare the defect distribution map acquired in Step 404 with the wafer test parameter distribution map acquired in Step 406 by utilizing an overlapping means. The number of overlapping dies is thus determined to calculate a ratio of the number of overlapping dies to the number of the failed dies. In this step, the number of overlapping dies is equal to the quantities of the defect dies and the failed dies in the overlapping portion. Step 408 is then executed to determine whether the ratio is greater than or equal to a predefined value or not, for example: 50%. If not, skip this layer. After all of the layers are skipped, stop analyzing. If

the ratio is greater than or equal to the predefined value, goes to Step 409.

[0037] In step 409, the product lot numbers, the data for the layers, and defect counts of the products, analyzed according to the above-mentioned analytical steps, are selected. In this preferred embodiment of the present invention, the layer analyzed according to the above-mentioned analytical steps is marked as a defective layer in this step. Then the lot of products including the wafer having the defective layer is searched to select the product lot number, the data for layers, and the count of defects.

[0038] Step 410 is executed to perform a statistical analysis. A representative value, being the kill ratio of the number of defects in the layer, is determined. Furthermore, the yield for products arriving at this layer in subsequent processes is forecasted according to the kill ratio and the method for analyzing defect inspection parameters in the preferred embodiment of the present invention.

[0039] In summary, the present invention method for analyzing the defect inspection parameters utilizes the commonality analysis means to analyze the defect inspection parameters, by coordinating with the database recording each defect inspection item and correlated processing equip-

ment. Therefore, the point which causes the problem to occur is judged rapidly and correctly to find out the ill-functioned equipment when the defect inspection data of semiconductor products indicates abnormalities. In addition, the kill ratio of the defect inspection is revised according to the results of defect inspection and wafer test to avoid mistakes incurred from human"s judgment, leading to higher processing efficiency, lower cost, and better in-line production status control to increase yield rate.

[0040] Those skilled in the art will readily observe that numerous modifications and alterations of the method may be made while retaining the teachings of the invention.Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.